

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

REMARKS

Claims 4 - 10, 12 - 15, 19, 20, 30 - 33 and 35 - 37 are pending in the above-identified application. Claim 20 is withdrawn from consideration.

In the Office Action of October 24, 2002, Claims 4 - 10, 12 - 15, 32, 33 and 36 were rejected. Claims 19, 30, 31, 35 and 37 were allowed. In response, Claims 4, 5, 8, 9, 10, 13, 14, 15, 32, 33 and 36 are canceled, Claims 6, 7 and 12 are amended and new Claim 38 is added to the application. (New Claim 38 is identical to Claim 2, which was previously canceled without prejudice or disclaimer.) Reexamination and reconsideration are respectfully requested in view of the foregoing amendments and the following remarks.

Amendments to Claims

The Examiner suggested corrections to Claims 4 and 7 to provide antecedent basis and to improve grammatical clarity. Accordingly, Claim 7 is amended to provide antecedent basis and improve grammatical clarity. (Claim 4 is canceled.) Because independent Claims 4 and 9 are canceled, dependent Claims 6, 7 and 12 are amended as independent claims.

New Claim 38 is identical to canceled Claim 2.

Rejection of Claims 4 - 10, 12 - 14 and 36 under 35 U.S.C. §103(a) over Yamazaki et al

Claims 4 - 10, 12 - 14 and 36 were rejected under 35 U.S.C. §103(a) as being obvious over Yamazaki et al (U.S. Patent No. 6,348,368). The Office Action alleges that Yamazaki discloses a crystallized active transistor layer with grains joined by {111} twin boundaries and describes the use of Pb as a catalytic agent to transform

amorphous material into a crystalline material. The Examiner further alleges that a gate electrode is mounted on the active layer via gate insulation layer since the product is TFT. Further, as to claims 4,14, the Examiner alleges that although the patent omits to disclose the claimed “alloys” of the agents as part of the agents, claim 3 indicates the possible existence of other associated materials or alloys with the agents by the expression “at least one selected from” to indicate material types associated with the agents. Therefore, the Examiner takes the position that it would have been obvious to one skilled in the art to conclude the existence of agent alloys in the crystallized TFT layer. As for claims 5,10,12, the Examiner alleges that since currents in TFTs travel through the channel, and that the channel is the crystallized TFT with the claimed crystal orientation, the claimed operation is met by the prior art. Further, the Examiner alleges that although the exact terminologies as that of the claim such as “dendryte” are not used, it is clear that there are crystallized regions in the active layer of the prior arts. As for claims 6,7, the Examiner alleges that the crystallizing agents of Yamazaki are oriented parallel to the substrate and that the claimed insulating substrates are also most common substrates in TFT formation. Further, the Examiner alleges that the plane orientation with {111} crystal-oriented layer is taught to be {110}. As for the claimed layer thickness or general layer dimension, the Examiner alleges that this is notoriously known as one of the most common variables that differ from a design to another based on an expected result. The Examiner further alleges that the magnitude given is also known to be within the range of “thin films” as understood in the art and that the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. The Examiner notes that where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a

claim, the applicant must show that the chosen dimensions are critical. As for the mobility of the active layer, the Examiner alleges that the element is again variable and heavily dependent on doping profile and concentration of crystallizing agents. Therefore, the Examiner takes the position that the claimed amount of mobility alone cannot be patented. Regarding claim 7, the Examiner alleges that the crystal grains in the active layers of the cited references are not restricted to a defined number and that therefore, it is clear that the claimed number of crystals is also covered in the references. As for claims 8,13, the Examiner alleges that no specifically unique physical substance can be deduced from the mathematical expressions unless fully detailed and shown by the applicant to contain something different from the thin film in the prior art. The Examiner takes the position that therefore, it is understood to be a similar film to that in the prior art. As for one structure on the polysilicon active layer in claim 7 is concerned, the Examiner alleges that both TFTs have gate insulation structures on the active layers and that as for said one point in claim 12, the crystals are finally connected to one another forming a larger crystal in such active layers. As for claim 9, the Examiner alleges that although the exact terminologies as that of the claim such as "dendryte" are not used, it is clear that there are crystallized regions in the active layer of the prior arts. As for the amorphous layer containing crystallizing agents, the Examiner alleges that crystallized layers are originally amorphous and metal agents are usually introduced to such layers in order to crystallize them, and that has already been addressed. As for claim 36, the Examiner alleges that metals are known gate materials.

This rejection is traversed as it may be applied to Claims 6, 7, 12 and new Claim 38. (Claims 4 - 5, 8 - 10, 13 - 14 and 36 are canceled.) The present invention of Claims 6, 7, 12 and 38 relates to a structure wherein the substrate has a {110}

orientation in addition to the grain boundaries having {111} twin crystals, as explained in more detail on page 8 of the specification and in embodiment 3 on page 13. Yamazaki discloses the crystallized active transistor layers having {111} twin-boundaries, but contrary to what is asserted by the Examiner, the reference contains no description or suggestion of other crystalline structures or crystalline orientation except {111}. In the present invention, on the other hand, the crystalline quality or crystalline structure is determined not only by the grain boundaries, but also by a substrate orientation. Yamazaki does not limit a substrate orientation, but only limits grain boundaries. Accordingly, it is respectfully submitted that Claims 6, 7, 12 and 38 would not have been obvious over Yamazaki.

Rejection of Claims 15 and 32 under 35 U.S.C. §103(a) over Yano et al

Claims 15 and 32 were rejected under 35 U.S.C. §103(a) as obvious over Yano et al (U.S. Patent No. 6,291,852).

This rejection is moot because Claims 15 and 32 are canceled herein.

Rejection of Claims 15 and 33 under 35 U.S.C. §103(a) over Yano in view of Yamazaki et al

Claims 15 and 33 are rejected under 35 U.S.C. §103(a) as obvious over Yano in view of Yamazaki. This rejection is moot because Claims 15 and 33 are canceled herein.

Conclusion

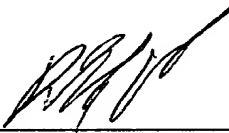
In view of the foregoing amendments and remarks, it is respectfully submitted that Claims 6, 7 and new Claim 38 are in condition for allowance, as well as allowed Claims 19, 30, 31, 35 and 37. Favorable reconsideration is respectfully requested.

Should the Examiner believe that anything further is necessary to place this application in condition for allowance, the Examiner is requested to contact applicants' undersigned attorney at the telephone number listed below.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (520.39251X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 
Ralph T. Webb
Reg. No. 33,047

Attachment: Marked-Up Copy To Show Changes Made

RTW/dlt
Tel.: (703) 312-6600
Fax: (703) 312-6666

MARKED-UP COPY TO SHOW CHANGES MADE

IN THE CLAIMS

6. (amended) A thin-film semiconductor device ~~as claimed in claim 4,~~
comprising an insulator, a polycrystalline layer formed on said insulator, and a
transistor comprising a source region, a drain region, a gate region, and a channel
region formed at the surface portion of said polycrystalline layer, said polycrystalline
layer comprising crystal grains of an element selected from the group of Type-IV
elements and their alloys, said crystal grains joined with crystal grain boundaries of
{111} twin of Diamond structure,

wherein said insulator is a glass substrate, said polycrystalline layer is a Si thin-film, said Si thin-film has a thickness of 10 to 150 nm, and said Si thin-film has a plurality of crystal grains having {110} planes parallel to the surface of said substrate.

7. (amended) A thin-film semiconductor device ~~as claimed in claim 4,~~
comprising an insulator, a polycrystalline layer formed on said insulator, and a
transistor comprising a source region, a drain region, a gate region, and a channel
region formed at the surface portion of said polycrystalline layer, said polycrystalline
layer comprising crystal grains of an element selected from the group of Type-IV
elements and their alloys, said crystal grains joined with crystal grain boundaries of
{111} twin of Diamond structure,

wherein in said channel region, the two to five crystal grains having the joints of said {111} twin have {110} planes parallel to the surface of said insulator, and have at least one structure coupled at one point on said polycrystalline layer.

12. (amended) A thin-film semiconductor device ~~as claimed in claim 9,~~
comprising an insulator, a semiconductor thin-film formed on said insulator and a
transistor comprising a source region, a drain region, a channel region and a gate
electrode formed at the surface of said semiconductor thin-film, said semiconductor
thin-film having amorphous regions of Type-IV element and dendrite crystal regions
of Type-IV element connecting said source region and said drain region,

wherein the two to five grains having the joints of {111} twins have {110}
planes parallel to the surface of said insulator and at least one structure coupled at
one point on said dendrite crystals, in said channel region.